Advanced Repeater Systems
D-Star® Repeater Controller
Installation and Operation Instructions

Overview

The ARS D-Star Repeater Controller (DRC) provides the necessary circuitry required for the reception and retransmission of 4.8 kbps Gaussian Minimum Shift Keying (GMSK) waveforms. The DRC utilizes the CML CMX589 GMSK modem integrated circuit phased locked loop (PLL) to acquire and lock on GMSK signals to less than 6 dB Signal to Noise. The DRC detects 4800 bit data patterns and generates a transmitter key (open collector, pull to ground). Data is delayed for approximately 250 mS to allow the repeater transmitter to stabilize and listening receivers to open so that header and data information is preserved. Data polarity is jumper selectable. Potentiometers set receive and transmit data levels. The controller may be used in conjunction with an analog or other digital mode repeater. Outputs are provided to indicate GMSK activity (active high) and to mute analog audio signals (via an AC-coupled shunt-to-ground transistor switch). Data is Gaussian shaped by a data pump, BT set to 0.5.

The data input requires direct connection to the receiver discriminator. The transmitter must be capable of Direct FM modulation. Generally any transmitter capable of Digital Code Squelch (DSC) should be capable of GMSK modulation. Many amateur radios that have a 9600 baud rate data port are also suitable.

The DRC does not decode or process (except delay and GMSK regeneration) any data. The DRC does not provide transmitter identification as required by the Federal Communications Commission Rules. If transmitter identification is required, it must be provided by the transmitter owner. This can be in the form of a traditional CW identification or in the digital transmission. If CW is used, the CW ID must wait for a data break and must stop when data is transmitted to prevent corruption of the data. There are commercial IDers available that have this “wait” feature. If the controller is part of a repeater system that includes a system controller, the identification passed from the system controller maybe sufficient.

Features & Specifications

- Small Size (2” x 2.75”) PCB
- DB-9 Male Connector
- Low Power (35 mA from 10 to 15 volt)
- Operation to less than 6 dB S/N
- Phased Lock Loop Data Detection
- Open Collector, Active Low Tx Key
- Rx and Tx Data Level Potentiometers
- Easy Interface with Double Face Tape
- PLL Free Run Mode for Fast Fade Recovery
- GMSK Transmits Data Pump set for BT=0.5
- LEDs for Power, S/N, Lock, Free Run, and Tx Key
- Activity and Mute Outputs for Dual Mode Operation
- 250mS Data Delay to allow Transmitter Stabilization

Operation

FM Noise and GMSK signals from the receiver discriminator are applied to the DRC Input. While receiving noise, the CMX-589 PLL is in a wideband, acquisition mode. During this time the Signal to Noise (S/N) LED flickers as it detects random but valid data crossings. When the CMX-589 detects a 4800 bps signal the control logic switches the PLL from wideband to narrowband to improve data tracking, key the transmitter, and light the Locked and Transmitter Key LEDs. The S/N LED brightens

with stronger signals, which corresponds to improved signal to noise conditions and improved bit-error-rates (BER). The recovered data is delayed by 250mS to allow the transmitter to stabilize and the listening receivers to open. The data is then run through a Gaussian (dual polarity, constant current source) data pump spectral shaping, buffered and filtered, then fed to the repeater transmitter.

If the signal fades the control logic places the PLL into a "Free Run" mode (lighting the F/R LED) for approximately 200 clock cycles which allows the recovery of data below 6 dB signal to noise until the signal either recovers or is lost in which case the PLL returns to the acquire mode.

Most of the DRC circuitry operates from an onboard five volt regulator with the exception of the output transmit data filter operational amplifier which operates from the supply voltage. This allows the DRC to drive loads that require up to seven volts peak to peak. Typical current draw is 35 mA from a 10 to 15 volt source. When the DRC is installed on a dual mode analog and D-Star repeater, it is suggested that the DRC be disabled by removing the power when operating in analog mode. The DRC power can be controlled from the repeater hang timer which should be controlled by a CTCSS or DCS decoder for the analog mode. Removing DRC power will prevent the DRC from responding to voice components which are sub harmonics of the 4800 data rate (i.e. 2400, 1200, 600, and 300 Hz).

The Controller has five LEDs to that provide Controller Status:

1. Power- Green indicates +5 volt present on the controller
2. Receive Signal to Noise (S/N)- intensity increases with signal
3. PLL Lock- Blue, indicates PLL is locked on Data
4. PLL Free Run- Blue, PLL lost lock due to weak or no signal and is "freewheeling" processing data below 6 dB S/N
5. Tx Key- Red, indicates that repeater transmitter is keyed

The Controller DB-9 Male Connector Pin Assignments:

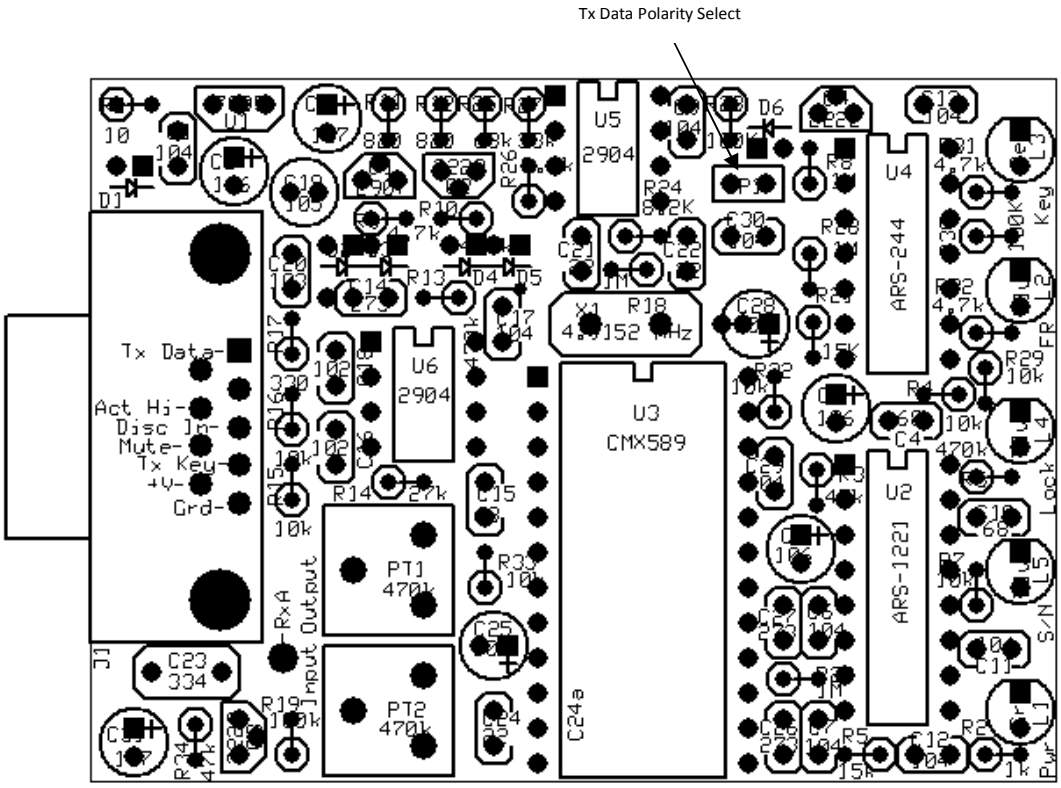
Pin 1	Transmitter Data Output
Pin 2	N/C
Pin 3	Receiver Discriminator Input
Pin 4	Transmitter Key (PTT)
Pin 5	Ground
Pin 6	N/C
Pin 7	Active High Logic Output
Pin 8	Tx Mute (to mute analog signals)
Pin 9	Supply Voltage Input

Installation

1. Identify a direct connector to the repeater receiver discriminator. If coupling capacitors are in the path, the corner should be less than 5 Hz. Higher corners will cause degraded performance and higher Bit Error Rate (BER) which may corrupt header data.
2. Identify a direct connector to the modulator suitable for GMSK data. Corners of DC blocking and coupling capacitors must be below 5 Hz to preserve transmits data and maintain a low talk-out BER.
3. Identify a suitable transmitter key that when grounded keys the transmitter.
4. Identify a clean positive 10 to 15 voltage source and ground point.
5. Identify a suitable location to mount the DRC. It should be away from high power RF and other sources of electrical noise.
6. If you are hard wiring (direct connect) the DRC, route wires directly to location of the controller while avoiding sources of RF and noise. Solder wires to the board using proper

ESD procedures (see drawing below). If using the DB-9 connector, do not solder the wires to the female connector while connected to the DRC.

7. Double check wiring before applying power to the DRC.
8. Turn on power, verify the Green power on LED is lit and the S/N LED is flickering.
9. Using a scope on the RxA test point, set the input potentiometer to 1 volt peak-to-peak data level with a D-Star input applied to the receiver.
10. Using a service monitor (or a listening analog receiver comparing the input to the output level) set the transmit data level to +/- 1.2 kHz deviation.
11. Using 2 D-Star Radios, verify that the radios communicate with each other through the repeater. If not, the data may be inverted. Remove the Tx Data Polarity Select jumper (see below) and verify proper operation.
12. Verify D-Star header call signs are properly being repeated. If header call signs are not being repeated but voice operation is normal, refer to the Troubleshooting Header Issues below.
13. System should now be operational.



Dual Mode Analog/D-Star Repeater Installation

When using the DRC on a dual mode repeater, analog signals such as voice, CW identification, CTCSS and DSC must be muted to prevent the corruption of the D-Star signal. The DRC provides two outputs which can be used to disable or mute signals- Pin 7 is an Active High CMOS indicator and Pin 8 is an AC coupled Audio Mute (pull to ground). Either or both can be used as required depending on the application.

As stated above, the best way to install the DRC on a dual mode repeater is to mute the Tx data from the DRC while operating in the analog mode. This prevents the DRC from corrupting analog signals when responding to voice sub-harmonics of the 4800 bps data rate.

However when the repeater is operating in the D-Star mode, incident analog signals must be disabled and muted from modulating the transmitter.

The Active High output (Pin 7) goes to a CMOS high (~5V) when the DRC detects a valid 4800 bps signal. This can be used to disable an analog transmit signal audio path via a transistor switch or CMOS analog mux or other circuitry. Be careful not to load this output, use a >10k series resistor.

The Audio Mute output (Pin 8) is an AC coupled mute which switches from a high impedance (47k ohms) to a low impedance (less than several ohms) when processing a D-Star signal. This should be installed on a high impedance audio point that mutes all analog signals (Tx Audio, CTCSS, etc.) without impacting the transmission of the D-Star data.

Troubleshooting Header Issues

Header call sign reception is vital in D-Star communications if you are linking your DRC equipped repeater with an ICOM D-Star repeater or compatible Hot-Spot. If your Repeater is passing voice communications and perhaps Tx messages but not passing header call signs; the received header is being corrupted either by a transmitter key transient or poor transmitter settling.

The DRC must have continuous discriminator noise applied at all times to ensure proper data acquisition and lock. Some radios create an unsquelch transient on the discriminator when a signal is received. Unsquelch the receiver (and turn receiver volume down) and verify if headers call sign is now properly repeated. If this solves the problem, either leave the receiver unsquelched or try moving the discriminator tap to a transient free location.

If the above did not solve the problem, it maybe a transmitter key transient caused when the transmitter keys. Continuously key the repeater transmitter using an external key or grounding the key line. Key the test D-Star Radio and verify if header call sign is properly repeated. If so, there is a voltage spike or sag caused when the transmitter keys. Check for ground loops.

Transmitter power amplifiers can consume large amounts of current which can cause voltage spikes and sags that impinge on sensitive frequency generator circuits of both Phase Locked Loops (PLL) and crystal oscillators which can cause brief frequency transients on the receiver while the header is being received. The best way to troubleshoot this is with an oscilloscope observing regulated voltages while keying and unkeying the transmitter. Many Motorola and GE mobile radio repeater conversions, which weren't design for full-duplex operation, suffer from voltage transients which impact the header. This can be resolved by isolating sensitive circuits with additional filtering and regulation which requires technical skill, documentation and test equipment to properly implement.

Poor Transmitter Settling

Data communications require transmitter frequency to be within +/- 250 Hz or less at the beginning of the data preamble and must have monotonic settling (free of ringing- frequency shifting up and down prior to final settling). This is a common problem with synthesized transmitters but can occur with crystal oscillators caused by ground loops and transient supply voltage spikes and sags which may be solved in the above. Synthesizer settling issues are caused by the design of the PLL loop dynamics which is beyond the scope of this manual.